IN THE CLAIMS

No claims are currently amended. The pending claim set is provided herein for the Examiner's convenience.

Claims 1-12. (Canceled)

13. (Original) A method of fabricating an integrated circuit package, comprising: mounting a thinned semiconductor die on a planar surface of a heat spreader.

14. (Original) The method of claim 13, wherein mounting includes mounting said die on to the heat spreader using a thermally conductive material.

15. (Original) The method of claim 13, wherein mounting includes attaching said die to the heat spreader by metal to metal diffusion bonding.

16. (Original) The method of claim 13, wherein said die has a thickness of no more than 100 μm.

17. (Original) The method of claim 13, further including forming at least one build-up layer over the die and heat spreader.

18. (Original) The method of claim 17, wherein forming includes emplacing a dielectric material to planarize exposed top surfaces of the heat spreader and the die.

19. (Original) The method of claim 18, wherein forming includes forming at least one build-up layer that includes at least one conductive trace contacting at least one contact on said die.

20. (Original) The method of claim 19, wherein forming includes forming at least two build-up layers, said at least two build-up layers including at least one dielectric layer disposed on at least a portion of the at least one conductive trace, and at least one second conductive trace extending through the at least one dielectric layer to contact the at least one conductive trace.

21. (Previously Presented) The method of claim 18, wherein forming a build-up layer includes emplacing the dielectric material by one of spin coating, curtain coating, slot coating, roll coating, squeegee application, or dry film lamination.

22. (Original) The method of claim 13, wherein said die is made thin by at least one of plasma etching, grinding, polishing, and chemical etching.

23. (Original) The method of claim 13, further comprising:
forming a metallization layer on said die.

24. (Previously Presented) A method of fabricating an integrated circuit package, comprising:
providing a planar heat spreader;
mounting a plurality of thinned semiconductor dice on to a planar surface of said heat spreader to form a plurality of conjoined microelectronic packages; and
singulating said plurality of conjoined microelectronic packages.

25. (Previously Presented) The method of claim 24, further including forming at least one build-up layer over top surfaces of the die and the heat spreader.

26. (Previously Presented) The method of claim 25, further including singulating said plurality of microelectronic packages by simultaneously cutting through said heat spreader and said at least one build-up layer.

27. (Previously Presented) The method of claim 25, further including forming a set of contacts to connect to an external component, the external component including a motherboard.

28. (Canceled)

29. (Previously Presented) The method of claim 24, wherein mounting includes mounting the plurality of semiconductor dice on to the heat spreader using a thermally conductive material.

30. (Previously Presented) The method of claim 29, wherein mounting includes forming a diffusion bond.

31. (Previously Presented) The method of claim 24, wherein said die has a thickness of no more than 100 um.

32. (Previously Presented) A method of fabricating an integrated circuit package, comprising:

mounting a thinned semiconductor die on a planar surface of a heat spreader, wherein the thinned semiconductor die has a thickness of no more than 100 μm, and wherein mounting includes:

depositing a metallization layer on a back surface of the die.

33. (Previously Presented) The method according to claim 32, wherein the metallization layer includes a plurality of sublayers.

34. (Previously Presented) The method according to claim 32, wherein the metallization layer includes a plurality of sublayers, selected from titanium, nickel, vanadium, and tin; titanium, nickel, vanadium, and gold; and titanium, nickel, vanadium, and tin and gold.

35. (Previously Presented) The method according to claim 32, wherein mounting is carried out by thermal bonding.

36. (Previously Presented) The method according to claim 32, wherein mounting includes forming a diffusion bond.

37. (Previously Presented) The method according to claim 32, further including:
forming at least one build-up layer over the die and heat spreader.

38. (Previously Presented) The method according to claim 32, further including:
forming at least two build-up layers over the die and heat spreader.

39. (Previously Presented) The method according to claim 32, wherein the thinned semiconductor die is one of a plurality of thinned semiconductor dice mounted on the planar surface of said heat spreader to form a plurality of conjoined microelectronic packages.

40. (Previously Presented) The method according to claim 39, further including:
forming at least one build-up layer that includes a conductive trace contacting at least one contact on one of said dice.

41. (Previously Presented) The method according to claim 39, further including:
forming at least one build-up layer that includes a conductive trace contacting at least one contact on one of said dice; and
singulating said plurality of conjoined microelectronic packages.

42. (Previously Presented) The method according to claim 41, wherein singulating includes singulating said plurality of microelectronic packages by simultaneously cutting through said heat spreader and said at least one build-up layer.

43. (Previously Presented) The method according to claim 39, wherein mounting includes mounting the plurality of semiconductor dice on to the heat spreader using a thermally conductive material.

44. (Previously Presented) The method according to claim 39, wherein mounting includes forming a diffusion bond.